Serial No.: 10/796,246
Docket No.: MIO 0069 VA

Remarks

Claim 23 has been added. Support for this claim is found in the specification and drawings, and thus no new matter has been added. Claims 2, 8, 16, and 23 are pending in the present application. Withdrawn claims 1, 3-7, 9-15, 17-23 and 22 are now canceled without prejudice.

Double Patenting Rejection

Claims 2, 8, and 16 have been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of Vaiyapura (U.S. 6,507,107) in view of Distefano (U.S. 6,075,289) and Suzuki (U.S. 5,532,910). Applicants respectfully traverse this rejection because the claims of the present invention are patentably distinct from the claims of the cited patents.

However, to simplify the issues in the present application, Applicants concurrently submit with this response the appropriate Terminal Disclaimer over Vaiyapura (U.S. Patent No. 6,507,107). In submitting this Terminal Disclaimer, Applicants state for the record that this Disclaimer is not an admission of obviousness in view of the cited U.S. patents. *Quad Envtl. Corp. v. Union San. Dist.*, 20 USPQ2d 1392 (Fed. Cir. 1991). Therefore, Applicants respectfully request withdrawal of the obviousness-double patenting rejections of claims 2, 8, and 16.

Rejection under § 103

Claims 2 and 8 have been rejected under § 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination with Distefano (U.S. 6,075,289) and Susuki et al. (U.S. 5,532,910). In addition, claim 16 has been rejected under § 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098), Distefano (U.S. 6,075,289) and Susuki et al. (U.S. 5,532,910) as applied to claim 2 and further in combination with Corisis et al. (U.S. 2002/0135066).

The Examiner stated that Lo teaches all the limitations of independent claims 2 and 8 except, in part, "a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate" or "at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling

capacitor is accommodated in a space." The Examiner further alleged that Distefano discloses a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone of the intermediate substrate and then concluded that it would have been obvious to one of ordinary skill in the art to incorporate a cap including a heat sink to the package of Lo to provide thermally enhanced packages as taught by Distefano. Also, the Examiner alleged that Suzuki utilizes a decoupling capacitor accommodated in a space coupled to a die and concluded that it would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including Lo in order to remove noise as taught by Suzuki.

Applicants respectfully disagree with these rejections and submit that the required prima facie case of obviousness has not been met. To establish a prima facie case of obviousness, three basic criteria must be met. *See* MPEP 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Independent claims 2, 8, and new claim 23 recite a printed circuit board assembly comprising, *inter alia*, a first semiconductor die, a second semiconductor die and an intermediate substrate positioned between the first semiconductor die and the second semiconductor die. The multiple die semiconductor assembly further comprises a heat sink including a cap thermally coupled to a major surface at least one of the semiconductor dies, wherein a peripheral portion of the cap engages a mounting zone defined by a lateral dimension of the intermediate substrate. As admitted by the Examiner, Lo "does not disclose[s] a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate." In an attempt to alleviate this deficiency in the primary reference (Lo), the Examiner alleged that Distefano's cap 22 could be incorporated into Lo's multi-chip package. Applicants respectfully disagree with this assertion.

Applicants submit that neither the references themselves nor the knowledge in the art provide sufficient motivation to incorporate Distefano's cap 22 into Lo's multi-chip package. The Federal Circuit has stated that if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Here, one of ordinary skill in the art could not incorporate Distefano's cap 22 into Lo's multi-chip package as claimed without rendering Lo's multi-chip package unsatisfactory for its intended purpose. First, the cap 22 cannot be placed over Lo's heat sink 50 and first semiconductor chip 26 in such a way that the cap 22 could be thermally coupled to a major surface of first semiconductor chip 26 (as recited in claims 2, 8, and 23) because the printed circuit board 100 is in the way and would have to be removed to permit such a configuration. Second, Distefano's cap 22 cannot be placed over Lo's second semiconductors 40 and 42 in such a way that the cap 22 could be thermally coupled to a major surface of second semiconductor chips 40 and 42 (as recited in claims 2, 8, and 23) because the encapsulant 46 is in the way and would have to be removed to permit such a configuration. If Lo's printed circuit board 100 or encapsulant 46 is removed, Applicants submit that Lo would be rendered unsatisfactory for its intended purpose.

Moreover, none of the references teach or suggest, singularly or in combination, the removal of Lo's printed circuit board 100 or encapsulant 46 in order to permit Distefano's cap 22 to be placed over Lo's heat sink 50 and/or semiconductor chips (26, 40, or 42) such that the cap may be thermally coupled to a major surface of these semiconductor chips. Thus, Applicants respectfully submit that one of ordinary skill in the art would have no reasonable expectation that such a modification or combination would provide any reasonable expectation of success. The Federal Circuit Court has stated, "Whether a particular combination might be 'obvious to try' is not a legitimate test of patentability." *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988) (citing *In re Geiger*, 815 F.2d 686, 688 (Fed. Cir. 1987).

Claim 8 also recites that the printed circuit board assembly comprises, *inter alia*, at least one decoupling capacitor mounted to a first surface of the intermediate substrate and conductively coupled to at least one of the first and second semiconductor dies. Lo is cited for teaching a multi-chip packaging structure having a first chip 26, second chips 40 and 42, and a substrate 10. The examiner concedes that Lo's structure fails to include decoupling capacitors.

To cure this noted deficiency, the examiner modifies the teachings of Lo by incorporating the decoupling capacitor of Suzuki into Lo's multi-chip packaging structure. The examiner asserted it would be obvious to incorporate the decoupling capacitor into the Lo structure to remove electric noise.

None of the cited references, singularly or in combination, teach all of the limitations of independent claim 8. Specifically, Suzuki teaches decoupling capacitors; however, Suzuki does not teach decoupling capacitors coupled to a first or second semiconductor die. The Suzuki decoupling capacitor is bonded to a conductive copper lead frame, not a semiconductor die. The placement of decoupling capacitors is essential for the functionality for the present invention. For example, each decoupling capacitor 60 may be placed in an electrical circuit between the high and low voltage inputs of one of the dies 20, 30. *See generally* [0028]. In this manner, the decoupling capacitors 60 decouple the low voltage input from the high voltage input on one of the dies, thereby serving as a power source filter or surge/spike suppressor. *Id.* Accordingly, the cited references, alone or in combination, fail to teach a decoupling capacitor coupled to a semiconductor die.

Furthermore, there is no reasonable expectation of success or motivation to combine the teachings of Lo and Suzuki in order to teach the invention recited in claim 8. As stated above, Suzuki teaches a decoupling capacitor bonded to a *conductive* copper lead frame. The prior art does not teach that incorporating the decoupling capacitor into a *semiconductor* die will have a reasonable expectation of success. Suzuki does not disclose that decoupling capacitors are effective at various voltages and currents. Moreover, the examiner asserts that Suzuki suggests the combination of Lo and Suzuki by stating that decoupling capacitors may remove electric noise. The Suzuki conductive lead frame may encounter electric noise, because it is an electrically conductive material. However, our invention does not disclose that electric noise is a problem to be resolved. If electric noise was a problem in our invention to be solved, one skilled in the art would resolve the electric noise problem at the source i.e. by coupling the decoupling capacitor to the conductive lines or frames. In contrast, semiconductor dies are less conductive than copper lead frames and will encounter less electric noise; therefore, one skilled in the art would not be led to couple the capacitors to semiconductor dies, as recited in independent claim 8. Thus, there is no motive to combine Lo and Suzuki, and there is no reasonable expectation of

success in modifying the Lo and Suzuki references to teach the invention as recited in independent claim 8.

Finally, claim 23 also recites that the printed circuit board assembly is configured such that the first and second semiconductor dies span the passage disposed within the intermediate substrate. Lo's first semiconductor chip 26 spans the passage 24, but as shown in Figure 1, neither of the second semiconductor chips (40 or 42) span the passage 24 as recited in Applicants' claim 23. In addition, none of the other references disclose or suggest, singularly or in combination, both semiconductor dies spanning a passage within an intermediate substrate of a printed circuit board assembly and thus do not teach or suggest all the limitations of Applicants' claim 23.

Therefore, the required burden of a prima facie case of obviousness has not been met and the Applicants respectfully request that the rejections under 35 U.S.C. §103 of independent claims 2 and 8 be withdrawn. As claim 16 depends from independent claim 2, the rejection under 35 U.S.C. §103 should be withdrawn as well. As set forth above, none of the references teach, singularly or in combination, teach all of the limitations of new claim 23, and thus it should be in condition for allowance as well.

Accordingly, the Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully requested.

Respectfully submitted,
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